SRI SAI RAM ENGINEERIG COLLEGE, CHENNAI – 44.
DEPARTMENT OF COMPUTER APPLICATIONS

Subject Code: MC1702 Subject Name : Microprocessors and Its Applications

16 Marks

1. Write in detail about the evolution of microprocessors.

History of Microprocessors

Name	Date	Transistors	Microns	Clock Speed	Data Width	MIPS
8080	1974	6,000	6	2 MHz	8 bits	0.64
8085	1977	~6200		3MHz- 5Mhz	8 bits	0.76
8088	1979	29,000	3	5 MHz	16 bits- 8 bit bus	2.5
80286	1982	1,34,000	1.5	6 MHz	16 bits	1
80386	1985	275,000	1.5	16 MHz	32 bits	5
80486	1989	1,200,000	1	25 MHz	32 bits	20
Pentium	1993	3,100,000	0.8	60 MHz	32 bits 64 bit bus	100
Pentium II	1997	7,500,000	0.35	233 MHz	32 bits 64 bit bus	~300
Pentium III	1999	9,500,000	0.25	450 MHz to 1 GHz	32 bits 64 bit bus	~510
Pentium 4	2000	42,000,000	0.18	1.5 GHz to 2.8 GHz	32 bits 64 bit bus	~1,700

2. What are the features of 8-bit microprocessors

Features of 8085 microprocessors

- It is an 8-bit microprocessor i.e. it can accept, process, or provide 8-bit data simultaneously
- It operates on a single +5V power supply connected at Vcc; power supply ground is connected to Vss.
- It has 16 address lines, hence it can access (216) 64 Kb of memory
- It provides 8 bit I/O addresses to access 256 I/O ports

- In 8085, the lower 8-bit address bus (A0-A7) and data bus (D0-D7) are multiplexed to reduce number of external pins. But due to this, external hardware (latch) is required to separate address lines and data lines.
- It supports 74 instructions with the following addressing modes: a) Immediate b) Register c) Direct d) Indirect e) Implied
- The Arithmetic Logic Unit (ALU) of 8085 performs:
  a) 8-bit binary addition with or without carry
  b) 16 bit binary addition
  c) 2 digit BCD addition
  d) 8-bit binary subtraction with or without borrow
  e) 8-bit logical AND, OR, EX-OR, Complement (NOT), and bit shift operations
- It has 8-bit accumulator, flag register, instruction register, six 8-bit general-purpose registers (B, C, D, E, H and L), and two 16-bit registers (SP and PC). Getting the operand from the general-purpose registers is faster than from memory.
- It provides 5 hardware interrupts: TRAP, RST 7.5. RST 6.5, RST 5.5 and INTR
- It has serial I/O control which allows serial communication
- It provides control signals (IO/M, RD, WR) to control the bus cycles, and hence external bus controller is not required.
- The external hardware can detect which machine cycle microprocessor is executing using status signals IO/M, S0, S1. This feature is very useful when more than one processors are using common system resources (memory and I/O devices).
- It has a mechanism by which it is possible to increase its interrupt handling capacity.
- The 8085 have an ability to share system bus with direct memory access controller. This feature allows to transfer large amount of data from I/O devices to memory or from memory to I/O device with high speeds

3. Write in detail about the architecture of 8085

Diagram of 8085 – 8 marks

Architecture of 8085

The various functional blocks are:

a) Registers
b) Arithmetic and Logic Unit
c) Instruction decoder and machine cycle encoder
d) Address buffer
e) Address/ Data buffer
f) Incrementor / Decrementor address latch
g) Interrupt control
h) Serial I/O control
i) Timing and control Circuit

Registers

It has eight addressable 8-bit registers: A, B, C, D, E, H, L, F and two 16-bti registers PC and SP. These registers can be classified as:

1. General Purpose Registers
2. Temporary Registers
   a) Temporary Data Register b) W and Z registers
3. Special Purpose Registers
   a) Accumulator b) Flag Registers c) Instruction Register
4. Sixteen bit Registers
   a) Program Counter (PC) b) Stack Pointer (SP)

General Purpose Registers

B, C, D, E, H and L are 8-bit general-purpose registers that can be used as separate 8-bit registers or as 16-bit register pairs BC, DE, and HL. When used in register pair mode, the high order byte resides in the first register and the low order byte in the second. HL pair also functions as a data pointer or memory pointer. These are also called scratchpad registers, as user can store data in them. To store and read data from these registers, bus access is not required as it is an internal operation.

Temporary Registers

a. Temporary Data register: The ALU has two inputs, one from the accumulator and other from temporary data register. The programmer cannot access this temporary data register. b. W and Z registers: They are used to hold 8-bit data during execution of some instructions and are not available for the programmer.

Use of W and Z instructions

1) The CALL instruction is used to transfer program control to a subprogram or subroutine. This instruction pushes the current PC contents onto the stack and loads the given address into the PC. The given address is temporarily stored in the W and Z registers and placed on the bus for the fetch cycle. Thus the program control is transferred to the address given in the instruction.
2) XCHG instruction exchanges the contents of H with D and L with E. At the time of exchange W and Z registers are used for temporary storage of data.

Special Purpose Registers:

1. Accumulator (Register A): It is a tri-state eight-bit register. It is extensively used in arithmetic, logic, load and store operations and I/O operations.

2. Flag Register. It is an 8-bit register, in which five of the bits carry significant information in the form of flags:

S	Z	X	AC	X	P	X	CY

S-Sign Flag: After the execution of arithmetic or logical operations, if bit D7 of the result is 1, the sign flag is set. In a given byte if D7 is 1, the number is viewed as negative number. If D7 is 0, it will be considered as positive number.

Z-Zero Flag: The zero flag sets if the result of operation in ALU is zero and flag resets if result is non-zero. The zero flag is also set if a certain register content becomes zero following an increment or decrement operation of that register.

AC- Auxiliary Carry Flag: This flag is set if there is an overflow out of bit 3 i.e., carry from lower nibble to higher nibble. This flag is used for BCD operations and it is not available for the programmer.

P-Parity Flag: the number of ones present in the accumulator defines Parity. After an arithmetic or logical operation if the result has an even number of ones i.e., even parity, the flag is set. If the parity is odd, flag is reset.

CY-Carry Flag: This flag is set if there is an overflow out of bit 7. The carry flag also serves as a borrow flag for subtraction.

3. Instruction Register: The Opcode of the instruction being processed is stored in this register.

Sixteen Bit registers

1. Program Counter (PC): It acts as a pointer to the next instruction; for one byte instruction it increments program counter by one, for two byte instruction it increments program counter by two and for three byte instruction it increments the program counter by three such that program counter always points to the address of the next instruction.

In case of JUMP and CALL instructions, address followed by JUMP and CALL instructions is placed in the program counter. The processor then fetches the next instruction from the new address specified by the JUMP or CALL instruction.

2. Stack Pointer: It holds the address of the most recent stack entry.

Arithmetic Logic Unit

8085's ALU performs arithmetic and logical functions on eight bit variables. The arithmetic unit performs bitwise fundamental arithmetic operations such as addition and subtraction. The logic unit performs logical operations such as complement, AND, OR and EX-OR, as well as rotate and clear. The ALU also looks after the branching decisions.

Instruction Decoder:

It decodes the instruction and accordingly gives the timing and control signals which control the register, the data buffers, ALU and external peripheral signals depending on the nature of the instruction.

Address Buffer: It is an 8-bit unidirectional buffer. It is used to drive external high order address bus. It is also used to tri-state the high order address bus under certain conditions such as reset, hold, halt and when address lines are not in use.

Address/ Data Buffer

It is an 8-bit bi-directional buffer. It is used to drive multiplexed address/data bus i.e., low order address bus (A7- A0) and Data bus (D7- D0). It is also used to tri-state the multiplexed address/data bus under certain conditions such as reset, hold, halt and when the bus is not in use.

The address and data buffers are used to drive external address and data buses respectively. Due to these buffers the address and data buses can be tri-stated when they are not in use.

Incrementer / Decrementer Address Latch

This 16-bit register is used to increment or decrement the contents of program counter or stack pointer as a part of execution of instructions related to them.

Interrupt Control

This block has five interrupt inputs RST 5.5, RST 6.5, RST 7.5, TRAP and INTR and one acknowledge signal INTA.

Serial I/O control

It provides two lines, SOD (Serial Output Data) and SID (Serial Input Data) for sending output data and receiving input data serially.

Timing and Control Circuitry

The control circuitry in the 8085 processor is responsible for all operations. The control circuitry and its operations are synchronized with the help of a clock. The operations are

- Control of fetching and decoding operations
- Generating appropriate signals for instruction execution and
- Generating signals required for interfacing external devices to the processor.

5.Write the pins and signals of 8085?

6.Explain in detail the instruction set of 8085.

7. Explain the interrupt structure of 8085.

8. Explain the timing diagram for Memory Read, Memory Write, I/O Read, I/O Write, Interrupt Acknowledge Machine Cycle, Opcode Fetch Machine Cycle.